ATTORNEY DOCKET NO. 068354.1443
CLIENT REFERENCE: MTI-1738.US.0

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	
Michael I. Catherwood	§	Group Art Unit: **2193**
	§	
Serial No.: **09/870,944**	§	
	§	Examiner: **Do, Chat C.**
Filed: **June 1, 2001**	§	
	§	
Title: **"DUAL MODE ARITHMETIC SATURATION PROCESSING"**	§	Atty. Docket No.: **068354.1443**

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF (37 C.F.R. § 41.37)

This Amended Brief is submitted in support of Applicants' Notice of Appeal from the rejections in the Final Office Action dated April 11, 2006 (the "Final Office Action") and the Notice of Panel Decision from Pre-Appeal Brief Review dated February 4, 2008.

I. IDENTIFICATION OF THE REAL PARTIES OF INTEREST

The real parties in interest is:

Microchip Technology Incorporated

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by virtue of assignments by the inventors as duly recorded in the Assignment Branch of the U.S. Patent and Trademark Office.

II. IDENTIFICATION OF RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences, to Applicants' knowledge.

III. STATUS OF THE CLAIMS

The application as originally filed contained 7 claims. Claims 1 and 3-5 are finally rejected and appealed. Claims 2, 6, and 7 were canceled. A listing of all appealed claims is provided in Appendix A in this Amended Brief.

IV. STATUS OF ANY AMENDMENT FILED SUBSEQUENT TO FINAL REJECTION

No amendment has been filed subsequent to final rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1 is directed to a system for overflow and saturation processing. (*See* Spec page 4, lines 6-19; Fig. 1, elements 10, 20, 30; Fig. 2, elements 20, 60, 65, 70, 75, 80, 90, 95, 150) The system includes an adder that is operatively connected to receive first and second operands, and connected to add the operands to produce a result of the added operands. (*See* Spec page 4, lines 6-13; page 5, lines 8-9; Fig. 1, element 30; Fig. 2, element 90). The system includes an accumulator that is operatively connected to store at least a portion of the result of the added operands or at least a portion of a selected one of predetermined constants based on control signals. (*See* Spec page 4, line 6-page 5, line 7; Fig. 1, element 10; Fig. 2, element 60) The system includes guard bits that are operatively connected to store the remaining portion of the result of the added operands or the remaining portion of the selected one of predetermined

constants based on the control signals. (*See* Spec page 4, line 20-page 5, line 2; page 5, lines 11-page 6, line 11, Table 1; Fig. 2, element 65) The system includes overflow logic that is operatively connected to the accumulator and to the guard bits so as to indicate overflow of the accumulator. (*See* Spec page 5, lines 3-6; Fig. 2, elements 70, 75, 80) The system includes saturation logic that is operatively connected to the adder, to the guard bits, and connected to provide the control signals based on at least a portion of the result of the added operands and at least a portion of the guard bits. (*See* Spec page 5, line 7-page 6, line 11, Table 1; Fig. 2, elements 20, 100, 105, 110, 115, 120, 125, 130, 135, 140, 145, 150) The system includes logic means for comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison. (*See* Spec page 6, line 3-page 7, line 5; Table 2; Fig. 2, element 95)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1 and 3-5 are patentable over U.S. Patent 4,945,507 issued to Ryuji Ishida et al. ("Ishida").

VII. ARGUMENTS

1. Claims 1 and 3-5 are patentable over Ishida

Claim 1 requires, in part, a system comprising "an accumulator, operatively connected to store at least a portion of the result of the added operands or at least a portion of a selected one of pre-determined constants based on control signals," "guard bits, operatively connected to store the remaining portion of the result of the added operands or the remaining portion of the selected one of predetermined constants based on the control signals," and "logic means for comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison."

Ishida discusses an overflow correction circuit for use in an arithmetic operation circuit. Specifically, Ishida discloses an adder 10 whose output 22 can be detected for an

overflow condition by detector 34. Depending upon the type of overflow condition, overflow detector 34 then directs the selector to forward one of three values (the maximum value 28, the minimum value 32 or the results of the adder 10) to the accumulator 46.

Ishida does not disclose each element of claim 1. For example, Ishida fails to teach a system for overflow and saturation processing comprising "**guard bits**, operatively connected to store **the remaining portion** of the result of the added operands or **the remaining portion** of the selected one of predetermined constants based on the control signals," as required by Claim 1. (emphasis added) Ishida discusses a method and system for detecting and correcting overflow in an arithmetic circuit (see Abstract) but does not store the result of the overflow. The present invention contemplates, *inter alia*, not only detection of overflow (e.g. overflow logic), but also storing of the overflow (*e.g.* guard bits), and detecting whether such overflow itself overflows (*e.g.* saturation logic).

The Final Office Action states that Ishida's D22 and D23 in Figure 2 disclose the "guard bits" of claim 1. (Final Office Action at 2-3) The Response to Arguments portion of the Final Office states that "Generally, the most significant bit(s) of adder 10 are considered as the guard bit(s), which is stored in flip-flop register 62 in Figure 2 or 6." (Final Office Action at 4) First, Applicant notes that claim 1 requires "guard bits," which are not disclosed by Ishida. The plurality of the guard bits is a limitation and cannot be read out of the claim. Applicant notes that there is only a single flip-flop register shown in each of Figures 2 and 6. With only a single register, the circuits can only store a single bit. Therefore Ishida's circuit in Figures 2 and 6 circuits do not disclose "guard bits . . . to store the remaining portion of the result," as required by the claim.

The mapping of Ishida to claim 1 becomes more strained when considering the limitation of "logic means for comparing **most significant bits of the guard bits and most significant bits of the result of the added operands**, and for generating the control signals in accordance with the comparison." The Final Office Action states that this limitation is also met by the circuit in Figure 2 and particularly by exclusive OR gate 66. (Final Office Action at 3) The inputs to the exclusive OR gate 66 are D22 and D23, which the Final Office Action earlier characterizes as the "guard bits." (Final Office Action at 2-3) The Final Office Action does not explain how the two-input exclusive OR gate 66 compares the most significant bits of the guard bits and most significant bits of the result of the added operands. The Final Office Action's mapping of these two sets of "most significant bits" reads at least one of them out of the claim by attempting to show that they are disclosed by the same element in Ishida. The rejection, therefore, is improper and fails to disclose this element. Applicant further incorporates the detailed arguments made with respect to this claim element in Applicant's Response to Final Office Action at pages 6-7.

For at least these reasons, Ishida does not disclose each element of claim 1. Claims 3-5 depend from claim 1 and are similarly patentable over Ishida.

VIII. SUMMARY

In light of the foregoing, Applicant respectfully requests that the final rejection of the pending claims should be reversed and the application be remanded for allowance of the pending claims, or, alternatively, remand the application for further examination if appropriate references can be found by the Examiner.

To the extent necessary, the Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0383, Order No. 063718.0773.

Respectfully Submitted,

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APPENDIX A: CLAIMS INVOLVED IN APPEAL

1. A system for overflow and saturation processing, comprising:

an adder, operatively connected to receive first and second operands, and connected to add the operands to produce a result of the added operands;

an accumulator, operatively connected to store at least a portion of the result of the added operands or at least a portion of a selected one of predetermined constants based on control signals;

guard bits, operatively connected to store the remaining portion of the result of the added operands or the remaining portion of the selected one of predetermined constants based on the control signals;

overflow logic operatively connected to the accumulator and to the guard bits so as to indicate overflow of the accumulator;

saturation logic, operatively connected to the adder, to the guard bits, and connected to provide the control signals based on at least a portion of the result of the added operands and at least a portion of the guard bits; and

logic means for comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison.

3. The system according to claim 1, wherein the saturation logic includes:

a selector operatively connected to selectively provide a one of the result of the added operands or a one of the predetermined constants based on the comparison.

4. The system according to claim 1, wherein the logic means includes:

means for providing the control signals in accordance with an enable signal and in accordance with the comparison.

5. The system according to claim 4, wherein the logic means further includes:

means, responsive to the comparison, for selectively providing the control signals so that the accumulator stores at least a portion of the result of the added operands and the guard bits store the remaining portion of the result of the added operands, or the accumulator stores at least a portion of a predetermined constant and the guard bits store the remaining portion of the predetermined constant.

APPENDIX B: EVIDENCE

None

APPENDIX C: RELATED PROCEEDINGS

None